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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/736,282	12/15/2000	Hideyuki Aoki	T&A-104	8133

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EXAMINER	
CHASE, SHELLY A	

ART UNIT	PAPER NUMBER
2133	10

DATE MAILED: 04/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/736,282	AOKI ET AL.	
	Examiner	Art Unit	
	Shelly A Chase	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44 & 50 to 52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14-22,36-44 and 52* is/are allowed.

6)☒ Claim(s) *1-13,23-35, 50 and 51* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Claims 1 to 44 and 50 to 52 are presented for examination.

Specification

2. The title of the invention is not precise. A new title is required that is clearly indicative of the invention to which the claims are directed.

3. The rejection of claims 23 to 30 and 32 to 35 was inadvertently omitted and should be rejected under 35 USC 103 as being obvious over Roy et al. in view of Momohara for the same rationale applied to claim 1.

4. The rejection of claims 1 to 13, 23 to 35 and 51 under 35 USC 103 as being obvious over Roy et al. in view of Momohara is **maintained** (see statutes in the first office action).

5. The rejection of claim 50 under 35 USC 102(e) as being anticipated over LeBlanc is **maintained** (see statutes in the first office action).

6. The rejection of claims 14 to 16, 18, 20 to 22, 36 to 39, 41 to 44, and 52 as being rejected under 35 USC 102 (e) over LeBlanc et al. is **withdrawn**.

7. The rejection of claim 17 as being obvious over LeBlanc in view of Ito et al. is **withdrawn**.

Claim Rejections - 35 USC § 103

8. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

9. Claims **23** to **30** and **32** to **35** are rejected under 35 U.S.C. 103(a) as being unpatentable over under 35 USC 103 as being obvious over Roy et al. in view of Momohara.

Claims **23** and **24**:

Roy substantially teaches the claimed invention. Roy does not specifically teach the data processing unit have a first memory mounted on it; however, Momohara in an analogous art teaches a method for testing semiconductor memory devices wherein a memory testing unit [100] includes a main memory [103] that stores the test program to test the semiconductor memory device (see col. 6, lines 27 to 35).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the tester of Roy to include a memory as taught by Momohara. This modification would have been obvious because a person of ordinary skill in the art would have been motivated to ensure the tester includes a storage device for storing instructions and test data to effectively test a semiconductor device.

As per claim **25**, Roy teaches testing a plurality of DUT's that are similar (see col. 3, lines 49 to 55).

As per claims **26** and **32**, Roy teaches the wafer includes a plurality of DUT (see fig. 2) and test data are applied simultaneously to the plurality of DUT's (see col. 5, lines 5 to 26).

As per claims **27** and **33**, Roy teaches a system controller [104] connected to the tester for controlling the test operations of the DUT; however fail to teach said data processing unit coupled to said first memory. Momohara teaches a CPU [102] connected to the main memory [103] (see fig. 8). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the test system of Roy to include a CPU connected to the main memory as taught by Momohara. This modification would have been obvious because a person of ordinary skill in the art would have been motivated to ensure the controller controls the memory for effectively testing the semiconductor device.

As per claims **28** and **34**, Roy teaches the interface circuitry comparing the expected data and data read from each DUT checking for mismatch (see col. 6, lines 10 to 19).

As per claims **29** and **35**, Roy teaches the test program creates a test program, test address, and other control signals ("clock signals and control signals"), (see col. 3, lines 55 to 60).

As per claim **30**, Roy teaches the DUt's are part of a semiconductor wafer (see col. 3, lines 57 to 60).

Allowable Subject Matter

10. Claims 14 to 22, 36 to 44, and 52 are allowed.

11. The following is an examiner's statement of reasons for allowance: the prior art of record teaches various methodologies of testing memory modules; however, the prior art made of record fail to teach or fairly suggest an apparatus and a method for testing a memory device, said apparatus comprising: a terminal supplied with a data processing unit having a memory mounted separately from said socket that supplies to said memory and that outputs signals of said memory. Claims 15 to 22 and 37 to 44 are directly dependent or indirectly dependent on claims 14 and 36 thus; these claims are allowable over the prior art made of record.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

12. Applicant's arguments filed 2-2-2004 with respect to claims 1 to 13, 23 to 35, 50 and 51 have been fully considered but they are not persuasive.

In response to the arguments concerning the previously rejected claims the following comments are made:

Applicants representative states that the Roy reference and Momohara reference fail to teach or fairly suggest " supplying at least one signal to a memory device to be tested and to a reference memory device in connection with the checking of the relationship between the output signals produced from the reference memory device and the output signals produced from the memory device to be tested." First, the examiner contends that the teachings of Roy in view of Momohara disclose supplying at least one signal to a memory device to be tested since, Roy in view of Momohara discloses a tester including a test sequence for testing a DUT ("memory device to be tested"), (see col. 5, lines 37 to 45).

Roy in view of Momohara also teaches using a single channel or multiple channels to test the DUT's (see col. 4, lines 48 et seq.). Thus, Roy in view of Momohara provides adequate support for the claimed limitation of supplying at least one signal to a memory device to be tested and has disclosed the claimed invention. Second, applicant appears to be arguing unclaimed features to the claim, the examiner cannot locate in independent claims 1, 9, 31 and 51 the limitation of "and to a reference memory device in connection with the checking of the relationship between the output signals produced from the reference memory device and the output signals produced from the memory device to be tested."

In response to the argument that the LeBlanc reference fail to teach "that the terminal supplied with a data processing unit has a memory that is mounted separately from the socket or board that is mounted with a memory device to be tested. The examiner agrees that the LeBlanc does not disclose the claimed feature; however the

feature is not claimed in independent claims 23 and 50 thus, LeBlanc provides adequate support for the claimed limitations as claimed in claims 23 and 50.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shelly A Chase whose telephone number is 703-308-7246. The examiner can normally be reached on Mon-Thur from 8:00 am to 6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shelly A Chase